Amendments to the Specification

Please replace the title with the following amended title:

CLOCK CONTROL CIRCUIT AND CLOCK CONTROL METHOD THAT SWITCHINGLY SUPPLIES A HIGH-SPEED CLOCK AND A LOW-SPEED CLOCK

Please replace the paragraph beginning on page 17, line 13 with the following amended paragraph:

The interrupt signal control section 30 is a structure for using an arbitrary signal from among a plurality of interrupt cause signals ~~INT1, INT2, ..., INTn~~, IN1, IN2, ..., INn, as the interrupt signal INT. The interrupt signal control section 30 has, in correspondence with the respective interrupt cause signals [[INTi]] Ini (i = 1~n), two-input ANDs 31i, and registers 32i setting whether or not the interrupt cause signals [[INTi]] Ini thereof are to be used. The interrupt signal control section 30 also has an n-input or 33 which is for outputting, as the interrupt signal INT, the logical sum of the output signals of these ANDs 31i. Note that, although not illustrated, the contents of the respective registers 32i can be set freely from the CPU 50.

Please replace the paragraph beginning on page 18, line 8 with the following amended paragraph:

The operation of this clock control circuit is the same as that of the clock control circuit in Fig. 1, except for the following points: by setting the registers [[31i]] 32i in the

interrupt signal control section 30, an arbitrary one of or an arbitrary plurality of the interrupt cause signals [[INTi]] INi can be used as the actual interrupt signal INT; and the speed of the high-speed clock HCK can be selected by the control signal C3 from the CPU 50.

Please replace the paragraph beginning on page 18, line 15 with the following amended paragraph:

As described above, because the clock control circuit of the second embodiment has the interrupt signal control section 30 and the high-speed clock source 40, in addition to the same advantages as in the first embodiment, there are the advantages that arbitrary interrupt cause signals [[INTi]] INi can be used, and that the speed of the high-speed clock HCK can be selected in accordance with the operational state.